International Application No.: PCT/JP2005/004337

U.S. Patent Application No.: Unknown

September 12, 2006

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IN THE ABSTRACT:

Please replace the Abstract of the Disclosure originally filed with the aboveidentified patent application with the following <u>new</u> Abstract of the Disclosure: International Application No.: PCT/JP2005/004337

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ABSTRACT OF THE DISCLOSURE

A semiconductor device includes, in first and second power source systems, electrostatic discharge (ESD) protective bonding pads connected by bonding wires to first and second power supply terminals and first and second ground terminals, first and second signal ESD protective element sections that are each connected to first and second signal bonding pads and the ESD protective bonding pads and protect first and second I/O circuits, respectively, and a power source ESD protective element section connected to first and second ESD protective bonding pads. The semiconductor device is capable of minimizing an increase in the chip size while implementing ESD damage countermeasures in which the power supply (or ground) terminal of one power source system serves as the reference potential terminal for the signal terminal of the other power source system.